ABSTRACT

Circuitry for reducing propagation delays in calculation of a value for use in a floating point multiply-accumulate operation. In the circuitry, a carry-save adder receives values of three input operands from three latches. A carry-lookahead adder receives the outputs from the carry-save adder and implements an XOR operation on a most-significant bit along with its own logic operation to produce a value for the floating point multiply-accumulate operation. Modification of the carry-lookahead adder to perform the XOR operation results in elimination of an entire stage of logic.